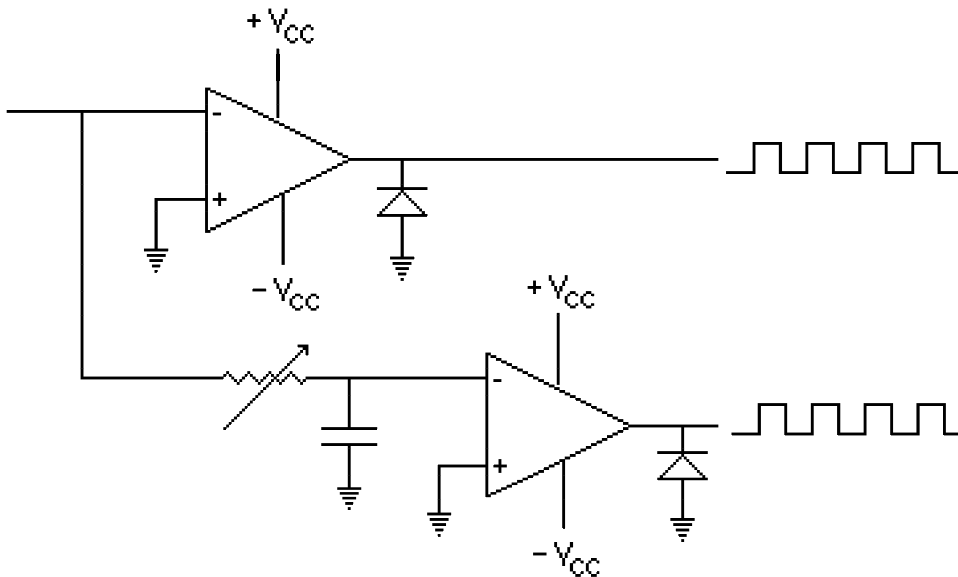


LABORATORY #4  
THE PHASE LOCKED LOOP

## EQUIPMENT

TL084 quadruple op amp  
7486 quadruple XOR (exclusive OR) gate  
74LS124 dual VCO (voltage controlled oscillator)  
5 V power supplies (2)

DEMONSTRATION OF A PHASE DETECTOR

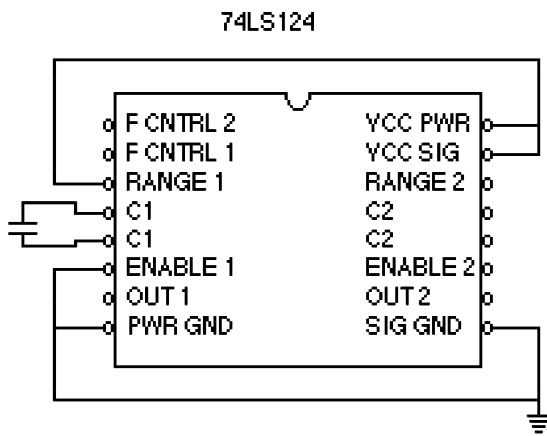
In order to test the phase detector which you are going to use in the phase locked loop (PLL) you will need a circuit which allows you to shift the phase of a signal. This is accomplished most easily by first shifting the phase of a sine wave, and then squaring it with an op amp used as a comparator. The circuit shown will yield square waves regardless of the shape of the input since the op amps will be driven between saturation and cutoff. The TL 084 op amp will use  $V_{CC}$  of 5 to 15 V. However, since you will be driving a TTL logic chip you will want to use 5 V. The pin diagram is the same as the 074 Quad amplifier which is shown in the manufacturer's spec sheets reproduced in the resource notebook, available in the lab. Use a sine wave input signal at a frequency around 10 kHz with no DC offset, and place each output on a channel of the oscilloscope to display the phase shift. Describe the function of the diodes. What is the maximum phase shift you can obtain from the circuit theoretically and in practice?

The phase detector that you will use is a simple XOR gate. The 7486 is a TTL chip so that you must use the fixed + 5 V output of your power supply for its  $V_{CC}$ . The pin diagram is also provided in the

bench notebook. Connect the two outputs of the above phase shifter to the "A" and "B" inputs of one of the XOR gates and monitor the output from the "Y" terminal on the oscilloscope. Explain the observed signal in terms of the logic chart for the XOR gate.

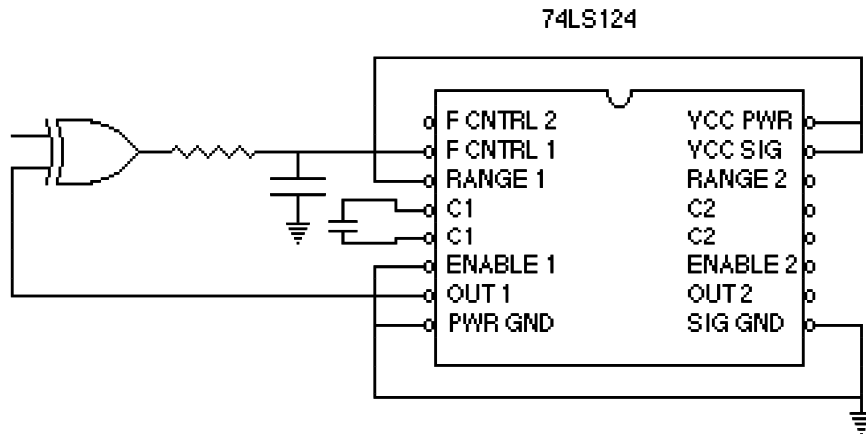
The output from the XOR will be averaged to provide a DC voltage that will control the frequency of the VCO. For this purpose you will use a simple RC filter as shown in the diagram below for the complete PLL. Describe how you choose a suitable RC combination. Measure and plot the DC voltage out of the XOR as a function of the phase difference between the two input signals. Describe how you measure the phase difference.

### OPERATION OF THE VOLTAGE CONTROLLED OSCILLATOR



The VCO pin diagram is as shown. A capacitor must be connected between the appropriate pins to set the center frequency of the oscillator. A  $0.01 \mu\text{F}$  capacitor will yield a frequency near 10 kHz with the control voltage near zero. The "range" input voltage controls how much the frequency will change for a given input voltage on the control line. For maximum variation connect this line to  $V_{CC}$  as shown. The oscillator is enabled with the enable line "low" or grounded. Both the signal  $V_{CC}$  and the power  $V_{CC}$  must be connected as well as their associated grounds. In order to estimate how well the PLL will lock to an input signal you will need to know the relationship between control voltage and frequency. Make a plot of these variables. Knowing this and the voltage range out of the phase detector, estimate the range of frequencies over which the PLL will lock on to a signal.

### CONSTRUCT THE PHASE LOCKED LOOP



Connect the XOR and VCO chips as shown. Connect the signal generator to the input of the XOR and monitor both this input and the signal out of the VCO on the scope. At the same time, monitor the DC voltage on the control line into the VCO. Tune the frequency of the signal generator until both signals on the scope are at the same frequency and phase locked. Describe how you use the scope sync to do this. When the signals are phase locked, measure the range of input frequencies over which the signal will remain phase locked (the "lock" range). Also measure the "capture" range, the high and low frequencies at which the PLL will lock in when approached from outside of the lock range. Does it make any difference which signal is connected to which input of the XOR? Can you explain why?

If you have difficulty obtaining a true phase lock, in which the control voltage varies smoothly with the input signal frequency, then the circuit is not functioning. If it is not working properly check all connections and recheck that both components work independently as they did in your first steps above.

### DEMODULATION OF AN FM SIGNAL

In this part of the experiment you will use the FG501A function generator as a frequency modulated input signal to the PLL. Start by determining the characteristics (output voltage, frequency, transfer function of the control voltage input in Hz/volt) of the FG501A before connecting it to the PLL. Set the frequency such that it is in the center of the range of the PLL. Use the other oscillator on your bench to generate a 10 Hz sine wave and connect it to the VCF (Voltage Controlled Frequency) input of the FG501A so as to modulate its frequency. Start with a small modulation such as a 1 V peak to peak signal, attenuated by 40 dB and monitor the output on the scope as you decrease the attenuation (increase the modulating voltage).

Finally, connect the FM signal to the input of the PLL and monitor the VCO control voltage on one

channel of the scope and the VCF input to the FG501A on the other channel. Describe what happens as the modulation is increased and decreased. Over what range of modulation amplitudes (frequency deviation) is the PLL a linear demodulator?