LABORATORY #2
TRANSISTOR AMPLIFIERS

Equipment

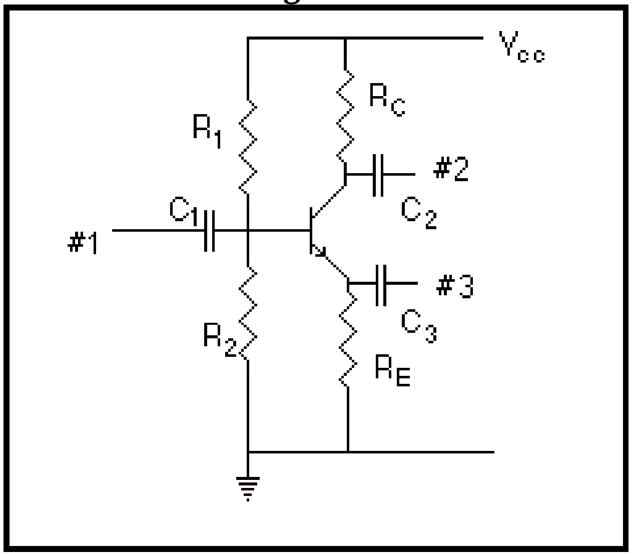
2N5210 NPN transistors
2N5484 N channel depletion mode JFET's
10 µFarad capacitors
47 µFarad capacitors
Resistance decade box and various resistors
(note that electrolytic capacitors must be connected with the correct polarity)

NOTES ON TECHNIQUE AND CONVENTIONS

V_{cc} or V_{dd} is supposed to be signal (AC) ground. To assure this, you should always bypass power connections at the circuit with a capacitor appropriate to the circuit. For audio frequencies, this usually means a large(≥10µF) electrolytic.Schematic diagrams usually omit this capacitor. In making connections to test equipment, take account of input and output impedances. Remember that coaxial cables are low impedance for short times; for long times, they look like capacitors of about 30pf/foot. Short refers to travel time in the cable, or about 1.4 nanoseconds/foot.

THE GENERIC BIPOLAR AMPLIFIER CIRCUIT

Figure 1



The circuit above can be easily converted into all three of the possible amplifier configurations. If R_E is bypassed, the amplifier becomes CE (common emitter). The input is at terminal #1 and the output at terminal #2. If R_c is shorted or bypassed, it becomes CC and the input is at terminal #1 with output at #3. If R_2 is bypassed it becomes CB with input at #3 and output at #2. We can not actually short the above terminals without altering the DC biasing that sets the operating point. However, if the capacitors, C_1 , C_2 , and C_3 are large enough, they can be used as AC short circuits. After you select values for the resistances as discussed in the next section, then decide how large each of these capacitors must be in order to function in this way assuming a signal frequency of 10 kHz. Because of the large capacitance required, electrolytic capacitors are commonly used at audio frequencies.

Setting the operating point.

Use your bench power supply to provide V_{CC}= 12 V. Use a self bias resistor $R_E \approx 300$ to 1000 Ω. From your previous measurements of the 2N5210 you should know that a reasonable operating current is 1 to 2 mA. In order to allow a usefully large voltage swing on the output you would like to have $V_{CE} \approx 0.6\ V_{CC}$. Choose your value of R_C accordingly. Since $V_{BE} \approx 0.6$ V, you can now determine the desired V_B and from this the desired ratio of R_1 / R_2. What is a reasonable criterion for the actual values of these resistors?

Measure each resistor that you select for the circuit to make certain that you have close to the desired value. Then assemble the circuit on your proto-board. Measure and adjust the power supply before connecting it to the circuit. With the circuit operating, use the DVM to check the voltages, V_{CE} , V_E , V_B . If they are not as desired, change the appropriate resistors to make them so.

Compute and measure the AC gain and its frequency dependence

For each of two circuit configurations (refer to Figure 1): 1) C_3 connected to ground (CE), 2) C_2 connected to ground (CC or emitter follower), use the small signal model to calculate the gain expected from the circuit with the values of the resistors you have used. Then apply a 10 kHz sine wave, between 0.01 and 0.1 V peak to peak, to the input and monitor both input and output on the oscilloscope to measure the gain. Determine the range of signal amplitudes over which the response is linear by increasing the input voltage until the output voltage is distorted. You will find this can be done very effectively by superimposing the two signals on the scope screen with their relative gains adjusted so as to produce exactly the same trace on the scope.

Increase and decrease the frequency of the input signal until the gain is decreased by $1/\sqrt{2}$. Record the frequencies of these half power points and estimate the phase shift between input and output from the two traces on the scope. In which configurations do you expect a 180^{o} phase shift in the mid frequency range? Calculate, from the component values used, the low frequency at which the gain drops to $1/\sqrt{2}$. The high frequency half power frequency is due to the internal design of the transistor.

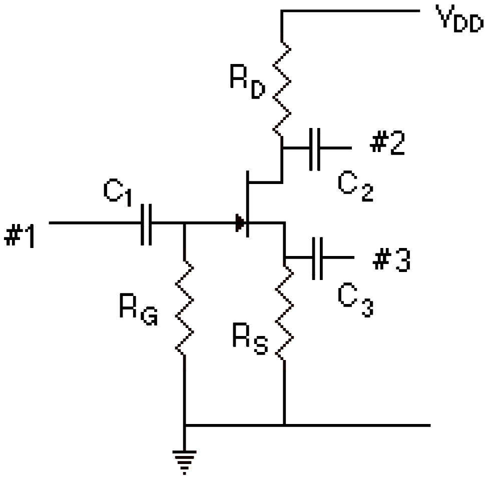
Measure the input and output impedance

For the same two circuit configurations, measure the input and output resistance at 10 kHz by connecting a resistance in series with the input and then in parallel with the output. The decade resistance box is very useful for this purpose since it allows you to find exactly the resistance at which the input or output signals are reduced by one half. Describe this process and the results. Do not use the definition Z_{out}=V(open circuit)/I(short circuit).

You lack a good way to measure AC current, and some circuit configutations (CE) cannot drive zero impedance.

THE GENERIC JFET AMPLIFIER

Figure 2



A general purpose circuit for an JFET amplifier, analogous to the bipolar transistor amplifier of figure 1, is shown in figure 2. This circuit takes advantage of the very high input impedance of the JFET as long as a large value resistor (say 1 megohm) is used for R_G.

Setting the operating point

Explain the self biasing scheme of this circuit. Again use a supply voltage V_{DD}=12V. Assume I_{DS} 1 mA and chose R_D so as to allow about a 6 V swing for the signal. Now use the decade resistance box for R_D and adjust it so that $V_D \approx 6$ V.

Measure the gain and its frequency dependence, and the input and output impedance

For the common source, and common drain (source follower) configurations measure the voltage gain at 10 kHz and find the high and low frequency half power points. Measure the input and output impedance. What value of g_m does your measured gain correspond to? Is its value consistent with other typical JFET's? Does the gain of the amplifier increase in proportion to R_D as in the small signal model?